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O García

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web the i 2c module contains an independent i 2c master logic and a i 2c slave logic which generates interrupts based

on their events in the multi master systems the user software is simply partitioned into the master controller and the slave controller when the i2c master logic is active the slave logic also remains active detecting the

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web i2c master h this header contains i o definitions selection and timing clock speed settings used for the master i2c interface this file also includes prototypes of master i2c functions i2c master c this source file contains master i2c function implementations file

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web i2c module modes and features the i2c module provides the following operational modes and features master mode slave mode with byte nacking multi master mode dedicated receive and transmit buffers up to four dedicated slave address registers 1

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web the i2c master is byte oriented and interrupt based the number of interrupts generated is kept at a minimum by automatic handling of most incidents the software driver complexity and code size are reduced by auto triggering of operations and a special smart mode which can be enabled by the smart mode enable bit in the control b register

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include sercom interrupt h define pinmux default 0

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web control of the i2c bus may be taken when the p bit is set or the bus is idle in firmware controlled master mode user code conducts all i2c bus operations based on start and stop bit condition detection start and stop condition detection is

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web lbidirectional i2c stands for inter integrated circuit communications i2c is implemented in the picmicro by a hardware module called the master synchronous serial port known as the mssp module

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 circuit more commonly referred to as i²c is a synchronous
 two wire bidirectional serial communications bus the i²c
 module can be used to communicate with other ic compatible
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 bidirectional master slave syn chronous interface between
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 these devices are connected via a two wire serial bus
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 integrated serial communications module the mssp contains
 two sub modules spi serial peripheral interface i²c inter
 integrated circuit the inter integrated circuit commonly

referred to as i²c is a synchronous two wire bidirectional
 serial communications bus

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web jun 23 2016 key features of the i²c module include the
 following independent master and slave logic multi master
 support which prevents message losses in arbitration detects
 7 bit and 10 bit device addresses with configurable address
 masking in slave mode detects general call addresses as
 defined in the i²c protocol automatic sclx clock

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web the i²c bus is a multi master serial data communication
 bus microcontrollers communicate in a master slave
 environment where the master devices initiate the
 communication and the devices are selected through
 addressing i²c operates with one or more master devices and
 one or more slave devices

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